IN THE SPECIFICATION:

Please replace paragraph 3 at page 10 continuing onto page 11, with the following rewritten paragraph:

FIG. 2 shows a configuration of then image-signal-holding portion 31. The image-signal-holding portion 31 writes the image signal DVu supplied from the input selection portion 21 into a memory and reads the image signal DVu written into this memory in synchronization with the image signal DVb. For example, three RAMs ~~312-a~~ 312-1 through ~~312-c~~ 312-3 are provided and a signal selector 311 is driven by the write control signal SEW, to sequentially allocate the image signals DVu to the RAMs ~~312-a~~ 312-1 through ~~312-c~~ 312-3 in frame units. Further, the write clock signal CKW is supplied to the RAM to which the image signal DVu is allocated, to store the allocated image signal DVu in the RAM. Further, the read clock signal CKR is supplied to the RAMs ~~312-a~~ 312-1 through ~~312-c~~ 312-3 to read the image signals DVu stored in the RAMs ~~312-a~~ 312-1 through ~~312-c~~ 312-3 in synchronization with the image signal DVb. Furthermore, a signal selector 313 is driven by the read control signal SER to select the read image signals DVu in order in which they were allocated and supply them as an image signal DVw to the mix-processing portion 41, the wipe-processing portion 42, and the output selection portion 43.

Please replace paragraph 1 at page 15, with the following rewritten paragraph:

When the three-frame sum signal is generated and then a frame of the image signal DVb is timed to start, for example, at time point t6 when the frame of the image signal DVb starts, the three-frame sum signal is read from the external read RAM and has its signal level multiplied by (1/3) and is output as the image signal DVb. Further, the frame from which the image signal DVb is generated by reading the three-frame sum signal from the external read RAM is specified

to be a frame of a valid image. It is to be noted if the three-frame sum signal is not completely written to the RAM yet or if a frame of the image signal DVb is timed to start when the three-frame sum signal is read completely, the image signal DVb of a previous frame is used repeatedly ~~and~~ so that the frame which is not completely written or is read completely, is rendered an invalid image frame. In this case, in the image signal DVb, no blank frame is provided between the image signals of a picked-up image of each frame.

Please replace paragraph 2 at page 16, with the following rewritten paragraph:

FIGS. 5A-5F explain operations of the frame rate conversion portion 30, for example, an operation where the frame rate of the image signal DVb is "60P" and that of the image signal DVu is "24P" as described above. It is to be noted that FIG. 5A shows frames of the image signal DVu, FIG. 5B shows an operation of an ~~RAM222-1~~ RAM312-1, FIG. 5C shows an operation of an ~~RAM 222-2~~ RAM312-2, FIG. 5D shows an operation of an ~~RAM222-3~~ RAM312-3, FIG. 5E shows frames of the image signal DVw, and 5F shows frames of the image signal DVb.

Please replace paragraph 1 at page 17, with the following rewritten paragraph:

At time point t11 shown in FIGS. 5A-5F when frame "F0" of the image signal DVu starts, the frame rate conversion portion 30 sets, for example, the RAM312-1 as a write RAM and supplies the image signal DVu to the write RAM using the signal selector 311, to store the image signal DVu of frame "F0" into the ~~RAM222-1~~ RAM312-1, which is the write RAM.